IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the Application:

LISTING OF CLAIMS:

1. (Currently Amended) A memory system, comprising:

a plurality of memory boards, each of the memory boards having a respective plurality of memory segments that may store respective data values, the segments being grouped into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer, the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments, the N respective segments in each respective parity set being distributed among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set, and a respective data value stored in a respective parity segment in at least one parity set may be calculated by a logical exclusive-or of respective data values stored in respective data segments in the at least one parity set, wherein:

each memory board includes a respective plurality of memory regions,

each memory region includes a respective subset of the segments included in a respective memory board, and

each of the segments included in a respective memory region may be assigned a respective base memory address different from other respective base

memory addresses that may be assigned to other segments included in the respective memory region.

2. (Original) The memory system of claim 1, wherein:

the number N is equal to 4.

Claim 3. (Canceled)

4. (Original) The memory system of claim 1, wherein:

the number N is equal to 4;

a respective data value initially stored in one respective data segment in the at least one parity set is equal to variable value A, and a respective data value initially stored in the respective parity segment in the at least one parity set is equal to variable value P;

the memory system includes circuitry that may be used to change the respective data values stored in the segments in the at least one parity set; and

when the circuitry is used to change the one respective data value from the variable value A to another variable value A', the circuitry also changes the respective data value stored in the respective parity segment in the at least one parity set from a variable value P to another variable value P', the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.

5. (Original) The memory system of claim 4, wherein the circuitry is configured to change, in respective atomic operations, the one respective data value and the respective data value stored in the respective parity segment in the at least one parity set.

6. (Original) The memory system of claim 1, wherein the memory boards comprise semiconductor memory, and each respective plurality of memory segments is comprised in the semiconductor memory.

7. (Currently Amended) A memory system, comprising:

a plurality of semiconductor memory segments, the segments being grouped into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer, the N respective segments in each respective group comprising respective data segments and a respective parity segment; and

in each of the groups:

the respective parity segment stores a respective data value P that may be calculated by a logical exclusive-or of respective data values stored in the respective data segments, wherein:

the segments reside in memory regions of a memory board, and

each of the segments included in a respective memory region may be assigned a respective base memory address different from other respective base

memory addresses that may be assigned to other segments included in the respective memory region.

8. (Original) The memory system of claim 7, wherein the plurality of memory segments are distributed among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group.

9. (Original) The memory system of claim 7, wherein:

the number N is equal to 4; and

in each of the groups:

the value P stored in the respective parity segment is equal to A XOR B XOR C, where A, B, and C are respective data values stored in the respective data segments, where "XOR" represents a logical exclusive-or function.

10. (Original) The memory system of claim 7, further comprising:

circuitry that may be used to implement an atomic operation by which one data value stored in one of the data segments in one of the groups may be changed from a first data value A to a second data value A', the circuitry also being usable to implement another atomic operation that changes to a data value P' the respective data value P stored in the respective parity segment in the one

of the groups, the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.

11. (Currently Amended) A method of using a memory system, the memory system including a plurality of memory boards, each of the memory boards having a respective plurality of memory segments that may store respective data values, the method comprising:

grouping the segments into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer, the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments;

distributing the N respective segments in each respective parity set among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set; and

storing in a respective parity segment in at least one parity set a respective data value that may be calculated by logically exclusive-or-ing together respective data values stored in respective data segments in the at least one parity set, wherein:

each memory board includes a respective plurality of memory regions;

each memory region includes a respective subset of the segments included in a respective memory board; and

each of the segments included in a respective memory region may be assigned a respective base memory address different from other respective base memory addresses that may be assigned to other segments included in the respective memory region.

12. (Original) The method of claim 11, wherein:

the number N is equal to 4.

Claim 13. (Canceled)

14. (Original) The method of claim 11, wherein:

the number N is equal to 4;

a respective data value initially stored in one respective data segment in the at least one parity set is equal to variable value A, and a respective data value initially stored in the respective parity segment in the at least one parity set is equal to variable value P; and

the method further comprises:

changing the one respective data value from the variable value A to another variable value A'; and

changing the respective data value stored in the respective parity segment in the at least one parity set from a variable value P to another variable

value P', the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.

15. (Original) The method of claim 14, wherein the changing of the one respective data value and the changing of the respective data value stored in the respective parity segment in the at least one parity set are executed in atomic operations.

16. (Currently Amended) The method of claim ~~1~~ 11, wherein the memory boards comprise semiconductor memory, and each respective plurality of memory segments is comprised in the semiconductor memory.

17. (Currently Amended) A method of using a memory system, the system comprising a plurality of semiconductor memory segments, the method comprising:

grouping the segments into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer, the N respective segments in each respective group comprising respective data segments and a respective parity segment; and

storing, in the respective parity segment in each of the groups, a respective data value P that may be calculated by logically exclusive-or-ing together respective data values stored in the respective data segments, wherein:

the segments reside in memory regions of a memory board of the system, and

each of the segments included in a respective memory region may be assigned a respective base memory address different from other respective base memory addresses that may be assigned to other segments included in the respective memory region.

18. (Original) The method of claim 17, wherein the method further comprises distributing the plurality of memory segments among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group.

19. (Original) The method of claim 17, wherein:

the number N is equal to 4; and

in each of the groups, the value P stored in the respective parity segment is equal to A XOR B XOR C, where A, B, and C are respective data values stored in the respective data segments, where "XOR" represents a logical exclusive-or function.

20. (Original) The method of claim 17, wherein the method further comprises:

executing an atomic operation that causes one data value stored in one of the data segments in one of the groups to be changed from a first data value A to

a second data value A', and also executing another atomic operation that changes to a data value P' the respective data value P stored in the respective parity segment in the one of the groups, the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.